Remarks

Claims 1–9, 45–55, and 59–67 are pending in this application. Claims 56–58 have been canceled. Claims 50–55 have been amended to make editorial changes. The amended claims are fully supported by the specification. No new matter has been added.

Section 112 Rejection

Claims 45–47. Claim 45–47 are fully supported by the specification. At paragraphs 6, 42, and 58–62, among other places, the application describes various implementations of the invention utilizing devices including DSPs. Some examples of DSP manufacturers listed include Texas Instruments, Analog Devices, and Motorola.

Some DSPs from these companies, as well as other DSP manufacturers, include the features recited in the claims. For example, Analog Devices manufactures a DSP family, ADSP-21xx, that with on-chip analog-to-digital converter (ADC). Texas Instruments has DSPs, such as the TMS320VC5507, TMS320VC5509, and TMS320C55x devices, with on-chip ADCs. See appropriate datasheets on DSP manufacturer's Web site.

Therefore, the specification contains a written description of the invention to enable a person skilled in the art to make and use the invention. The examiner should withdraw the section 112, first paragraph rejection. Since these claims were not otherwise rejected, these claims are now in a form for allowance.

Claims 61–63. Claim 61–63 are fully supported by the specification. For example, figure 4 of the application shows a phase-locked loop (PLL) block which is below the L2 memory 1024K bytes block, identified by reference number 408. Figure 6 shows a PLL block below the M2 RAM block, identified by reference 620.

Therefore, the specification contains a written description of the invention to enable a person skilled in the art to make and use the invention. The examiner should withdraw the section 112, first paragraph rejection. Since these claims were not otherwise rejected, these claims are now in a form for allowance.

Claims 50–55. Claims 50–55 are related to the claims from they depend. Since these claims were not otherwise rejected, these claims are now in a form for allowance.

Section 103 Rejection

Claims 1–6, 8–9, 48, and 59–60 have been rejected under section 103 as being unpatentable over U.S. patent publication 2003/0152084 (Lee). Claims 7, 49, and 64–67 have been rejected under section 103 as being unpatentable over Lee, as applied to claims 1–6 and 8–9 above, and further in view of U.S. patent 6,769,033 (Bass). Reconsideration of the rejection and allowance of the claims are respectfully requested.

No Prima Facie Showing of Obviousness (Argument 1)

For the reasons given in applicants' May 29, 2008 response, the applicants continue to believe claims 1–9, 48, and 59–60 are allowable over the cited references. In particular, for example, claim 1 recites "receiving incoming traffic from the network *in a digital signal processing integrated circuit having at least 128K bytes of on-chip memory*." Lee and Bass, considered individually or in combination, do not show or suggest a digital signal processing integrated circuit or DSP.

In fact, the cited references exemplify the shortcomings of the prior art. Lee describes using a custom multiple instruction single data (MISD) processor. Lee, paragraphs 69–75. And not just one such MISD integrated circuit, but multiple MISD integrated circuits connected together (i.e., figure 4 shows three MISD processors chips connected together). In fact, Lee *teaches away* from using a DSP. At paragraph 8, Lee states:

> Given the ever increasing bandwidth demand, RISC processors should be removed from the data path because they are not designed to optimally process the high-bandwidth data traffic coming from network equipment. Currently, RISC processors are being used as graphics processors and digital signal processors ("DSPs") and have been tailored to meet the demands of these applications. Unfortunately, the general nature of network traffic processing is completely different than graphics processing or digital signal processing and the RISC processor architecture, which is based on techniques created decades ago, becomes a big burden for network traffic processing. For example, in a DSP, the execution unit is processing at a rate that is orders of magnitude faster than the data it is executing (i.e., the execution unit can easily process the incoming data). In other words, the data is relatively static in comparison to the execution unit.

> This is the case in both graphics and digital signal processing. In contrast, the information, data, voice and video entering at the ingress of a network processor is traveling at a very high speed and the growth rate of the line rate is in correlation with the bandwidth demand curve.

Clearly, Lee teaches against the use of DSPs in network processing and is quite the opposite of the claimed invention. Lee would definitely not suggest putting four MISDs together into a single DSP. Bass also does not show or suggest DSPs for network processing. Therefore, the examiner has not given a *rational underpinning* to support a conclusion of obviousness. Rather, the examiner is making conclusory statements. For at least this reason, all claims should be allowable.

Prior Art Falls Short: No DSP Integrated Circuit (Argument 2)

Claim 1 recites "receiving incoming traffic from the network in a *digital signal processing integrated circuit* having at least 128K bytes of on-chip memory." Lee never describes using a DSP integrated circuit for network processing.

In contrast to the invention, Lee describes a custom designed integrated circuit or chip (referred to as a MISD processor) for network processing, rather than using an off-the-shelf part such as a DSP. Designing a custom integrated circuit from scratch involves specifying the chip, designing the chip, laying out the chip, making the masks for the chip, fabricating the chip, testing the ship, debugging the chip, and making revisions to the masks in the case that the chip does not function or operate properly.

The invention uses a digital signal processing (DSP) integrated circuit to manage network processing. In figures 4–6 and at paragraphs 57–59, the application describes some specific implementation using DSP integrated circuits from, for example, Texas Instruments, Analog Devices, and Motorola. As one of skill in the art can appreciate, there is much less complexity and lower cost when using DSPs to perform network processing as compared to the Lee approach of design a custom integrated circuit.

For at least this reason, claim 1 should be allowable.

Not Four Cores on Single Integrated Circuit (Argument 3)

Further, claim 1 recites digital signal processing (DSP) integrated circuit with "a *first core*," "a *second core*," "a *third core*," and "a *fourth core*," each performing a function of the

managing traffic technique and these *four cores residing on the same integrated circuit.* Nowhere does Lee show or suggest an integrated circuit with four cores. In figure 4, Lee provides three MISD processors as separate integrated circuits. Separate integrated circuits are very different from single integrated chip (e.g., see figure 6 of the application which shows a DSP integrated circuit with multiple cores).

Based on the examiner's position with respect to the present claims, some extremely important inventions would not be patentable today. An example is the invention of the integrated circuit which is the joining of two transistors together on a single substrate. At that time, the integrated circuit was patented by Jack Kilby (i.e., U.S. Patent 3,115,581 for "Miniature Semiconductor Integrated Circuit") at Texas Instruments and Robert Noyce at Fairchild Semiconductor. In fact, Jack Kilby won the Nobel Prize in Physics in 2000 for his invention of the integrated circuit. The integrated circuit has been recognized by people around the world as a great and worthy invention.

So too, the applicants believe the present invention to be an important contribution to the progress of the useful arts. If applicants are not allowed patent protection, applicants will not have the incentive to be creative and innovative. For at least this additional reason, claim 1 should be allowable.

Congestion and Scheduling Not in Separate Cores (Argument 4)

Further, claim 1 recites "performing a *congestion control function in a second core*" and "*scheduling function in a third core.*" Lee does not show or suggest this feature.

Specifically, Lee describes that the scheduling and congestion control functions are preformed simultaneously in a single core (called the storage congestion metering unit). Lee, paragraphs 361–362, and figures 4 (i.e., MISD processor 220b) and 34 (showing details of MISD processor 220b). Lee states that "incoming information element may be discarded based on the drop probability and the scheduling entry for the particular class to which the flow of the incoming information element belongs." Paragraph 362. The storage congestion metering unit includes a class storage unit which includes a scheduling entry that specifies one or more information element arriving at different position that are to be discarded and then the discard scheduler can discard these information elements are incoming. Paragraph 362. Whether to accept or discard the incoming information element is specified by the discard scheduler.

Paragraph 363. As figure 34 indicates, the discard schedule is dependent on the class characteristic storage unit which holds the scheduling information.

Therefore, the congestion function is dependent on the scheduler function, so these cannot be split into separate cores (and is a reason why Lee does not need more than three cores—another reason why the examiner has not made a proper *prima facie* showing of obviousness). For at least this additional reason, claim 1 should be allowable.

Prior Art Has Scheduling Before Congestion (Argument 5)

Further, claim 1 recites "wherein the *third core processes data generated by the second core*." As discussed above, Lee does not show or suggest congestion and scheduling performed by separate cores. And further, in Lee, the scheduling function is performed before congestion function. Paragraphs 361–362 and figure 34. This is different from what is claimed because the third core *processes data generated by the second core*. For at least this additional reason, claim 1 should be allowable.

Claims 2–7, 45, 48–50, 53, 61, 64, and 65 are dependent on claim 1 should be allowable for at least similar reasons as claim 1. These dependent claims recite additional limitations which further distinguish the invention over the cited reference.

Claims 8–9 should be allowable for at least similar reasons as discussed above. Dependent claims 46–47, 51–52, 54–55, 59–60, 62–63, and 66–67 should be allowable for at least similar reasons as the claim from which they depend.

Conclusion

For the above reasons, applicants believe all claims now pending in this application are in condition for allowance. Applicants respectfully requests that a timely Notice of Allowance be issued in this case. If the examiner believes a telephone conference would expedite prosecution of this application, please contact the signee.

Respectfully submitted,

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